

What Is Claimed Is:

1 1. An apparatus for generating quadrature phase
2 signals, comprising:
3 a base selector having a control input terminal for
4 receiving a region control signal, a plurality of reference
5 clock input terminals respectively for receiving a
6 plurality of reference clock signals of the same frequency
7 and different phases, and four base clock output terminals
8 for outputting a first, a second, a third and a fourth base
9 clock signals, said first, said second, said third and said
10 fourth base clock signals being generated in accordance
11 with said region control signal by using said plurality of
12 reference clock signals, a phase difference between said
13 first and said second base clock signals being
14 substantially equal to a phase difference between said
15 third and said fourth base clock signals, a phase difference
16 between said first and said third base clock signals being
17 substantially 90 degrees, a phase difference between said
18 second and said fourth base clock signals being
19 substantially 90 degrees;
20 a first phase interpolator having a control input
21 terminal, two phase input terminals for respectively
22 receiving said first and said second base clock signals,
23 and a first output terminal, said first phase interpolator
24 generating a first clock signal at said first output
25 terminal in accordance with a position control signal at
26 said control input terminal, said first clock signal having
27 a frequency equal to the frequency of said first and said
28 second base clock signals and having a phase being a weighted
29 average of the phases of said first and said second base
30 clock signals; and
31 a second phase interpolator having a control input

32 terminal, two phase input terminals for respectively
33 receiving said third and said fourth base clock signals,
34 and a second output terminal, said second phase
35 interpolator generating a second clock signal at said
36 second output terminal in accordance with a position
37 control signal at said control input terminal, said second
38 clock signal having a frequency equal to the frequency of
39 said third and said fourth base clock signals and having
40 a phase being a weighted average of the phases of said third
41 and said fourth base clock signals, said first and said
42 second clock signals being substantially 90 degrees out of
43 phase with each other.

1 2. The apparatus for generating quadrature phase
2 signals of claim 1, wherein said first, said second, said
3 third and said fourth base clock signals are generated by
4 selecting four signals from said plurality of reference
5 clock signals and their inverted signals.

1 3. The apparatus for generating quadrature phase
2 signals of claim 1, wherein said base selector has four
3 reference clock input terminals for receiving four
4 reference clock signals, the phases of said four reference
5 clock signals and their inverted signals are offset from
6 one another by 45 degrees, and said first, said second, said
7 third and said fourth base clock signals are generated by
8 selecting four signals from said four reference clock
9 signals and their inverted signals.

1 4. The apparatus for generating quadrature phase
2 signals of claim 3, wherein the phase difference between
3 said first and said second base clock signals is
4 substantially 45 degrees and the phase difference between

5 said third and said fourth base clock signals is
6 substantially 45 degrees.

1 5. An apparatus for generating quadrature phase
2 signals, comprising:

3 a base selector, comprising:

4 a buffer/inverter unit having four input terminals,
5 four corresponding control terminals and four
6 corresponding output terminals, said buffer/inverter
7 unit receiving a first, a second, a third and a fourth
8 reference clock signals of the same frequency and
9 different phases respectively at said four input
10 terminals and outputting four signals selected from said
11 first, said second, said third and said fourth reference
12 clock signals and their inverted signals respectively
13 at said four corresponding output terminals based on
14 control signals at said four corresponding control
15 terminals; and

16 a bypass/cross unit including a first and a second
17 bypass/cross multiplexers, each of said multiplexers
18 having two input terminals, two output terminals and a
19 control terminal, said first bypass/cross multiplexer
20 having its two input terminals connected to two of said
21 four output terminals of said buffer/inverter unit and
22 outputting a first and a third base clock signals by
23 either direct-connecting or cross-connecting signals
24 at its two input terminals to its two output terminals
25 in accordance with a control signal at its control
26 terminal, said second bypass/cross multiplexer having
27 its two input terminals connected to the other two of
28 said four output terminals of said buffer/inverter unit
29 and outputting a second and a fourth base clock signals

30 by either direct-connecting or cross-connecting
31 signals at its two input terminals to its two output
32 terminals in accordance with a control signal at its
33 control terminal, a phase difference between said first
34 and said second base clock signals being substantially
35 equal to a phase difference between said third and said
36 fourth base clock signals, a phase difference between
37 said first and said third base clock signals being
38 substantially 90 degrees, a phase difference between
39 said second and said fourth base clock signals being
40 substantially 90 degrees;

41 a first phase interpolator having a control input
42 terminal, two phase input terminals for respectively
43 receiving said first and said second base clock signals,
44 and a first output terminal, said first phase interpolator
45 generating a first clock signal at said first output
46 terminal in accordance with a position control signal at
47 said control input terminal, said first clock signal having
48 a frequency equal to the frequency of said first and said
49 second base clock signals and having a phase being a weighted
50 average of the phases of said first and said second base
51 clock signals; and

52 a second phase interpolator having a control input
53 terminal, two phase input terminals for respectively
54 receiving said third and said fourth base clock signals,
55 and a second output terminal, said second phase
56 interpolator generating a second clock signal at said
57 second output terminal in accordance with a position
58 control signal at said control input terminal, said second
59 clock signal having a frequency equal to the frequency of
60 said third and said fourth base clock signals and having
61 a phase being a weighted average of the phases of said third

62 and said fourth base clock signals, said first and said
63 second clock signals being substantially 90 degrees out of
64 phase with each other.

1 6. The apparatus for generating quadrature phase
2 signals of claim 5, wherein said buffer/inverter unit of
3 said base selector comprises a plurality of XOR
4 (Exclusive-Or) gates.

1 7. The apparatus for generating quadrature phase
2 signals of claim 6, wherein said buffer/inverter unit of said
3 base selector comprises four XOR (Exclusive-Or) gates, each
4 having two input terminals, respectively used as one of said
5 four input terminals of said buffer/inverter unit for
6 receiving one of said reference clock signals and as one of
7 said four corresponding control terminals of said
8 buffer/inverter unit for receiving one of said corresponding
9 control signals.

1 8. The apparatus for generating quadrature phase
2 signals of claim 5, wherein the phases of said first, said
3 second, said third and said fourth reference clock signals
4 and their inverted signals are offset from one another by
5 45 degrees.

1 9. The apparatus for generating quadrature phase
2 signals of claim 8, wherein the phase difference between said
3 first and said second base clock signals is 45 degrees and
4 the phase difference between said third and said fourth base
5 clock signals is 45 degrees.

1 10. A data recovery circuit, comprising:
2 a phase detector receiving an incoming data signal and
3 a first and a second clock signals, said first and said second

4 clock signals having a frequency equal to half the frequency
5 of said incoming data signal and being substantially 90
6 degrees out of phase with each other, said phase detector
7 comparing the phase of said incoming data signal with the
8 phase of said second clock signal and accordingly generating
9 a phase error signal if a phase difference exists between
10 said incoming data signal and said second clock signal while
11 generating an output data signal recovered from said
12 incoming data signal with said first clock signal if no phase
13 difference exists between said incoming data signal and said
14 second clock signal;

15 a loop filter receiving said phase error signal from said
16 phase detector and accordingly generating a region control
17 signal and a position control signal for adjusting the phases
18 of said first and said second clock signals;

19 a multiphase clock source for generating a plurality of
20 reference clock signals of the same frequency and different
21 phases from an external clock signal; and

22 a quadrature phase generator receiving said region
23 control signal and said position control signal from said
24 loop filter and said plurality of reference clock signals
25 from said multiphase source and generating said first and
26 said second clock signals for outputting to said phase
27 detector, said quadrature phase generator comprising:

28 a base selector for generating a first, a second, a
29 third and a fourth base clock signals in accordance with
30 said region control signal by using said plurality of
31 reference clock signals, a phase difference between said
32 first and said second base clock signals being
33 substantially equal to a phase difference between said
34 third and said fourth base clock signals, a phase
35 difference between said first and said third base clock

36 signals being substantially 90 degrees, a phase
37 difference between said second and said fourth base clock
38 signals being substantially 90 degrees;

39 a first phase interpolator receiving said first and
40 said second base clock signals and generating a first
41 clock signal in accordance with said position control
42 signal, said first clock signal having a phase being a
43 weighted average of the phases of said first and said
44 second base signals; and

45 a second phase interpolator receiving said third and
46 said fourth base clock signals and generating a second
47 clock signal in accordance with said position control
48 signal, said second clock signal having a phase being a
49 weighted average of the phases of said third and said
50 fourth base signals.

1 11. A data recovery circuit, comprising:

2 a phase detector receiving an incoming data signal and
3 a first and a second clock signals, said first and said
4 second clock signals having a frequency equal to half the
5 frequency of said incoming data signal and being
6 substantially 90 degrees out of phase with each other, said
7 phase detector comparing the phase of said incoming data
8 signal with the phase of said second clock signal and
9 accordingly generating a phase error signal if a phase
10 difference exists between said incoming data signal and
11 said second clock signal while generating an output data
12 signal recovered from said incoming data signal with said
13 first clock signal if no phase difference exists between
14 said incoming data signal and said second clock signal;

15 a loop filter receiving said phase error signal from said
16 phase detector and accordingly generating a region control

17 signal and a position control signal for adjusting the
18 phases of said first and said second clock signals;
19 a multiphase clock source for generating a first, a
20 second, a third and a fourth reference clock signals of the
21 same frequency and different phases from an external clock
22 signal; and
23 a quadrature phase generator receiving said region
24 control signal and said position control signal from said
25 loop filter and said four reference clock signals from said
26 multiphase source and generating said first and said second
27 clock signals for outputting to said phase detector, said
28 quadrature phase generator comprising:
29 a base selector, comprising:
30 a buffer/inverter unit receiving said four
31 reference clock signals and selectively outputting
32 four signals selected from said first, said second,
33 said third and said fourth reference clock signals
34 and their inverted signals respectively at its four
35 output terminals in accordance with said region
36 control signal; and
37 a first and a second bypass/cross multiplexers,
38 said first bypass/cross multiplexer generating a
39 first and a third base clock signals by either
40 direct-outputting or cross-outputting signals at
41 two of the four output terminals of said
42 buffer/inverter unit in accordance with said region
43 control signal, said second bypass/cross
44 multiplexer generating a second and a fourth base
45 clock signals by either direct-outputting or
46 cross-outputting signals at the other two of the four
47 output terminals of said buffer/inverter unit in
48 accordance with said region control signal, a phase

49 difference between said first and said second base
50 clock signals being substantially equal to a phase
51 difference between said third and said fourth base
52 clock signals, a phase difference between said first
53 and said third base clock signals being
54 substantially 90 degrees, a phase difference between
55 said second and said fourth base clock signals being
56 substantially 90 degrees;

57 a first phase interpolator receiving said first and
58 said second base clock signals and generating a first
59 clock signal in accordance with said position control
60 signal, said first clock signal having a phase being a
61 weighted average of the phases of said first and said
62 second base signals; and

63 a second phase interpolator receiving said third and
64 said fourth base clock signals and generating a second
65 clock signal in accordance with said position control
66 signal, said second clock signal having a phase being
67 a weighted average of the phases of said third and said
68 fourth base signals.

1 12. The data recovery circuit of claim 11, wherein said
2 buffer/inverter unit of said base selector comprises four
3 XOR (Exclusive-Or) gates, each having two input terminals
4 respectively for receiving one of said reference clock
5 signals and for receiving one bit of said region control
6 signal.

1 13. The data recovery circuit of claim 11, wherein the
2 phases of said first, said second, said third and said fourth
3 reference clock signals and their inverted signals are
4 offset from one another by 45 degrees.

1 14. The data recovery circuit of claim 13, wherein the
2 phase difference between said first and said second base
3 clock signals is substantially 45 degrees and the phase
4 difference between said third and said fourth base clock
5 signals is substantially 45 degrees.

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